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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,643	11/15/2000	John E. Gavlik	P04762	3643

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EXAMINER	
PATEL, ASHOKKUMAR B	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/713,643	GAVLIK ET AL.	
	Examiner	Art Unit	
	Ashok B. Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are subject to examination.

Response to Arguments

2. Applicant's arguments filed July 06, 2004 have been fully considered but they are not persuasive for the following reasons:

Referring to claims 1, 9, and 17,

a. In response to applicant's arguments against the references individually (references Cooper as well as Johnson), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

b. In response to Applicant's arguments that "In addition, the Office Action asserts that a person skilled in the art would combine Cooper With Johnson because it would allow the controller of Cooper to update the "status of the subroutines" and to check the subroutine's "progress of execution because if one subroutine fails to terminate the microcontroller becomes incapable of executing any further instructions." (Office Action, Page 4, First paragraph). However, Cooper already recites a mechanism for tracking the status of subroutines (various flags) and a mechanism for identifying and terminating subroutines that have hanged (various timers). (col. 3, lines 39-65.,. Col. 4, Line 66 - Col. 5, Line 84. As a result, there is no need to modify Cooper as suggested in the Office Action because Cooper already includes the functionality forming the basis for combining Cooper with Johnson.", first of all, the office action specifically describes

the microcontroller capabilities by stating " microcontroller which is capable of....." that are taught by the reference Cooper. These capabilities are of the important relevancy to the elements of the claim 1, 9 and 17 as stated in the office action. The reference Cooper's teachings regarding the multitasking control program (firmware instructions, task initialization and service routines) is not explicitly taught as claimed, that is exactly what is stated in the office action by stating "Although, Copper teaches, the first memory includes microcontroller firmware instructions, task initialization and service routines, it fails to explicitly teach multitasking control program comprising a main routine and a plurality of subroutines callable by the main routine, and a routine of first memory calling a subroutine and upon encountering a decision point that is not yet capable of being decided, updates the vector with the address of decision point associated with the subroutine and transferring the program execution control back to the main routine.", that necessitates the explicit teachings of the reference Johnson as stated in the office action by being motivated as stated by the reference Cooper which is also stated in the office action.

The teachings of the reference Johnson that considered are, as stated in the office action, "The reference Johnson teaches the process (main routine) comprising of a collection of procedures (a plurality of subroutines), each performing some subtask of the process. The reference goes on teaching that the process for the needed data can call these procedures where the data is exchanged via stack (memory data structure) (col.4, lines 60-68 and col.5, lines 1-24). The reference also teaches that the procedure can be placed into dormant state (a decision point that is not yet capable of being

decided) and the status message of the procedure is updated (updating the vector of the subroutine) and then the process can resume another procedure by calling and transitioning to execution state. After the completion of another procedure, the process can come back to the dormant procedure to continue the execution from where it left the procedure. (col. 7, lines 10-68 and col.8, lines 1-28, Figs.) and 5)." which has no relevancy to whether the "process (main routine) comprising of a collection of procedures" is executed on one processor or multiple processors, which is being argued by the applicant by stating ""purpose of Johnson, which renders Johnson unsuitable for its intended purpose. Because the whole purpose of Johnson is to execute. a process using multiple processors."

The same is true that Johnson lacks the teachings of Cooper, i.e. Microcontroller and its capabilities, and as such by following Cooper's suggestion "where the status of the subroutines is updated periodically for coming back to check it's progress of execution because if one subroutine fails to terminate the microcontroller becomes incapable of executing any further instructions", as stated in the office action, one having ordinary skill will combine the teachings of the references.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having

ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper (US 6,182,238) in view of Johnson et al. (hereinafter Johnson) (US 4,530,051).

Referring to claims 1 and 2,

The reference Cooper teaches the buses to which the microcontroller can be connected such as peripheral component interface (PCI) or special purpose buses, thereby the reference suggests that the microcontroller can be used on a network interface card providing an interface between the network and the PCI bus. (Fig. 1 and col.5, lines 28-33). The reference also discloses microcontroller which is capable of executing multitasking control program (firmware instructions, task initialization and service routines) with first memory (ROM 200) capable of storing multitasking control program including service routines, and second memory (RAM 202) capable of storing plurality of multitasking vectors (operational parameters, task execution flags, task status flags) associated with multitasking control program (firmware instructions, task initialization and service routines). Also the reference teaches the communication taking place between the first memory (ROM 200) and the second memory (RAM 202) (col.3, lines 15-65 and Fig. 2). Although, Copper teaches, the first memory includes microcontroller firmware instructions, task initialization and service routines, it fails to explicitly teach multitasking control program comprising a main routine and a plurality of subroutines callable by the main routine, and a routine of first memory calling a subroutine and upon encountering a decision point that is not yet capable of being decided, updates the

vector with the address of decision point associated with the subroutine and transferring the program execution control back to the main routine. The reference Johnson teaches the process (main routine) comprising of a collection of procedures (a plurality of subroutines), each performing some subtask of the process. The reference goes on teaching that the process for the needed data can call these procedures where the data is exchanged via stack (memory data structure) (col.4, lines 60-68 and col.5, lines 1-24). The reference also teaches that the procedure can be placed into dormant state (a decision point that is not yet capable of being decided) and the status message of the procedure is updated (updating the vector of the subroutine) and then the process can resume another procedure by calling and transitioning to execution state. After the completion of another procedure, the process can come back to the dormant procedure to continue the execution from where it left the procedure. (col. 7, lines 10-68 and col.8, lines 1-28, Figs.) and 5). Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a network interface card with a microcontroller including multitasking control program comprising the main routine and a plurality of subroutines callable by main routine in the first memory as taught by the references and providing multitasking vectors in the second memory associated with the multitasking control program where the status of the subroutines is updated periodically for coming back to check it's progress of execution because if one subroutine fails to terminate the microcontroller becomes incapable of executing any further instructions as taught by Cooper.

Referring to claims 3, 4, 5 and 6,

The reference Cooper teaches the first memory as being a read-only memory (ROM) (Fig.2, element 200), the second memory as being a random access memory (RAM) (Fig.2, element 202), and both, ROM and RAM memories are internal to the microcontroller (Fig.2). The reference also teaches ROM as being an external device coupled to microcontroller through secondary bus. (Fig. 1, elements 102, 134 and 124).

Referring to claims 7 and 8,

The reference cooper teaches that the components such as dispatch and watch dog timers can be incorporated within the microcontroller or be external to the microcontroller. It also teaches that a computer processor can also perform the methods performed by the microcontroller. It also teaches the various memory storage devices that may be used with a microcontroller. (col.5, lines 26-42). Thereby, it teaches that the first memory and second memory needed for storing and executing the microcontroller control program routines and subroutines (microcontroller firmware instructions, task initialization and service routines) may be RAM or ROM or a combination of both, which can be externally or internally coupled to a microcontroller.

Referring to claims 9 and 10,

Claims 9 and 10 are rejected for the reasons set forth for the claims 1 and 2, and the reference Cooper's teaching of a processing system including a data processor. (Fig. 1 element 104).

Referring to claims 11, 12, 13 and 14,

Claims 11, 12, 13 and 14 are rejected for the reasons set forth for the claims 3, 4,

5 and 6.

Referring to claims 15 and 16,

Claims 15 and 16 are rejected for the reasons set forth for the claims 7 and 8.

Referring to claims 17 and 18,

Claims 17 and 18 are the methods of the claims 1 and 2. Therefore claims 17 and 18 are rejected for the reasons set forth for claims 1 and 2.

Referring to claims 19, 20, 21 and 22,

Claims 19, 20, 21 and 22 are the methods of the claims 3, 4, 5 and 6. Therefore claims 19, 20, 21 and 22 are rejected for the reasons set forth for claims 3, 4, 5 and 6.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (703) 305-2655. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (703) 305-8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abp
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JOHN FOLLANSBEE
SUPERVISORY PATENT E...
TECHNOLOGY CENTER 2100